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D. Remarks

Rejection of Claim 5 Under 35 U.S.C. §112, Second Paragraph.

Claim 5 has been amended to address this ground for rejection.

Rejection of Claims 1-3, 5 and 21-22 Under 35 U.S.C. §103(a), based on U.S. Patent No. 5,780,910 (*Hashimoto et al.*) in view of U.S. Patent No. 6,750,113 (*Armacost et al.*)

The invention of claim 1 is directed to a memory cell that includes a first node for storing a first potential, a second node for storing a second potential, transistor gate electrodes formed from a gate layer, and a capacitor having plates coupled between the first node and second node. A portion of one plate of the capacitor comprises a first interconnect wiring pattern that includes a plurality of conductive layers. The plurality of conductive layers are commonly etched into the same pattern with substantially aligned edges.

To establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[1]

As emphasized above, Applicants claim 1 recites a portion of one plate of a capacitor comprises a first interconnect wiring pattern, where such a wiring pattern includes a plurality of conductive layers "commonly etched into the same pattern with substantially aligned edges". Such an arrangement is not shown or suggested by the cited combination of references.

The rejection notes that *Hashimoto et al.* fails to show a "plurality of conductive layers commonly etched into the same pattern with substantially aligned edges".[2] To show such limitations, the rejection looks to *Armacost et al.*:

> Armacost et al. disclose a capacitor comprising a plurality of conductive layers commonly etched into the same pattern with substantially aligned edges. *See at least Figs 1-2, for example, Cols. 1-2, lines 66-67, 1-51, respectively, and the related disclosure.* (See the Office Action, dated 06/01/2007, Page 5, Lines 6-8).

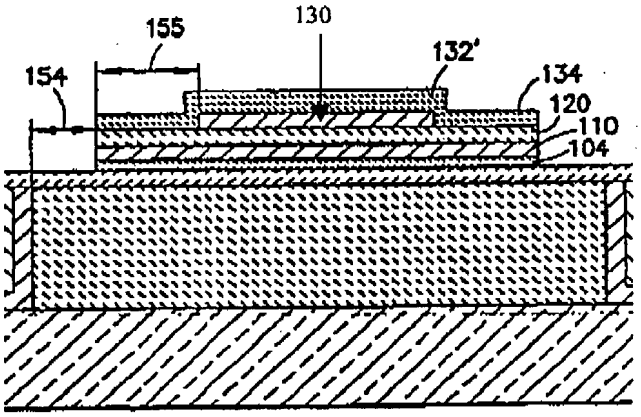
[1] MPEP §2143.
[2] See the Office Action, dated 06/01/2007, Page 5, Lines 4-5.

Applicants respectfully disagree with this interpretation of the cited reference.

Not only does *Armacost et al.* not teach "substantially aligned edges", but the reference appears to expressly teach away from such a limitation.

Armacost et al. shows a metal-insulator-metal capacitor that can be included within a copper manufacturing technology. The capacitor shown has only two conductive layers, a bottom plate layer (110) and a top plate layer (130). These layers are intentionally patterned so as to not have aligned edges:

> Another feature of the invention is the provision of ***a capacitor top plate*** that does not include copper and ***is smaller on all sides than the bottom plate.*** (*Armacost et al.*, Col. 1, Lines 31-33, emphasis added).



The edges of bottom plate (110) are not aligned with those of top plate (130).

Applicants note that the etched bottom plate (110) of *Armacost et al.* is aligned with layer (104), as shown in FIG. 3 of the cited reference above. However, layer (104) is not a conductive layer, but rather an insulating layer of silicon dioxide.

> An initial capacitor stack includes first (nitride Si_3N_4) cap layer 102 (advantageously part of the regular metallization), ***sacrificial (oxide SiO_2) layer 104***, bottom plate layer 110... (*Armacost et al.*, Col. 2, Lines 7-9, emphasis added).

Accordingly, because the cited combination of references does not show all the limitations of claim 1, and the reference relied upon is believed to teach away from such limitations, a prima facie case of obviousness has not been established.

For this reason alone, this ground for rejection is traversed.

In addition or alternatively, Applicants do not believe sufficient motivation has been presented for combining *Hashimoto et al.* in view of *Armacost et al.*, as proposed by the rejection. In combining *Hashimoto et al.* in view of *Armacost et al.*, the rejection argues the following:

> It would have been obvious... to modify Hashimoto as taught by Armacost et al. in order to prevent early wearout or potential breakdown. (See the Office Action, dated 06/01/2007, Page 5, Lines 9-12).

Applicants believe that this rationale is not sufficient to establish a prima facie showing.

Armacost et al. is concerned about early wear out and potential breakdown – the exact issue noted by the rejection. But the reference teaches that this problem arises for a very specific reason: the inclusion of copper interconnects in a device.

> In the field of copper interconnect, however, development of a suitable process has proved to be unexpectedly difficult. The potential hillocks and gouges in a copper metal surface can cause thinning and discontinuities in the active dielectric or in the capacitor plates, ***leading to early wear out and potential breakdown.*** (*Armacost et al.*, Col. 1, Lines 14-20, emphasis added).

Thus the rejection rationale for combining/modifying *Hashimoto et al.* in view of *Armacost et al.* appears to arise out of the problems related to copper interconnect emphasized by *Armacost et al.*

However, *Hashimoto et al.* provides no teachings related to copper. In fact, copper is never mentioned in the reference.[3] Thus, because *Hashimoto et al.* does not include copper, Applicants do not believe it would be obvious to one skilled in the art would to incorporate a structure for countering the effects of copper, as proposed by the rejection. That is, one skilled in the art would not be motivated to find solutions to a non-existent problem.

Accordingly, because the proposed rationale for combining the references does not appear sufficient for a prima facie case, this ground for rejection is traversed for this additional reason.

Equally well settled is the standard for patentability with respect to obviousness enunciated by the Supreme Court of the United States.

> Under § 103, the scope and content of the prior art are to be determined; differences between the prior art and the claims at issue are to be ascertained; and the level of ordinary skill in the pertinent art resolved. Against this background, the obviousness or nonobviousness of the subject matter is determined... As indicia of obviousness or nonobviousness, these inquires may have relevancy...[4]

Applicants believe that the above factors also illustrate how the invention of claim 1 is nonobvious. As noted from the above discussion, the cited references not only fail to show an arrangement where "conductive layers are commonly etched into the same pattern with substantially aligned edges", but *Armacost et al.* teaches away from such a limitations. Further, because the capacitor of *Armacost et al.* is effective for use in processes with copper interconnects, there is nothing presented by the references or the rejection that provides a reason for utilizing such a structure in a process without copper interconnects (i.e., that of *Hashimoto et al.*). Absent such a reason, Applicants do not believe a prima facie case of obviousness can be established.

Various claims depending from independent claim 1 are believed to be separately patentable over the cited reference. Arguments directed to selected dependent claims are set forth below. The separate patentability of these claims should not be construed as implying that other dependent claims are not believed to be separately patentable.

Claim 5, which depends from claim 1, recites that the first interconnect wiring layer pattern includes a plurality of separate portions, each portion including a bottom conductive layer, a dielectric layer formed over the bottom conductive layer, and a top conductive layer formed over the dielectric layer. The bottom conductive layer forms at least a portion of a first plate of the capacitor. The bottom conductive layer, dielectric layer, and top conductive layer have the same pattern.

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[3] A word search of *Hashimoto et al.* for "copper" or "Cu" yields no matches.

[4] Graham v. John Deere, 383 U.S. 1 (1966). See also M.P.E.P. §2141.

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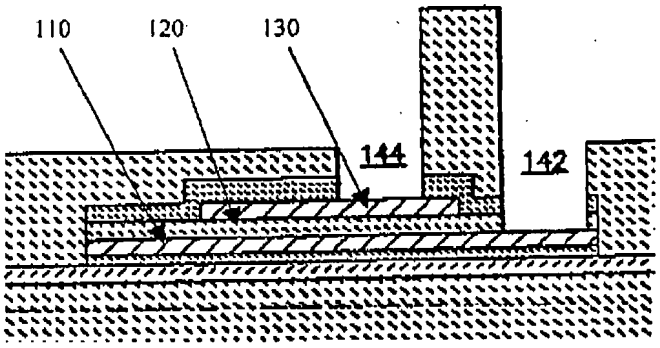
To show the limitations of claim 5, the rejection relies on the same rationale as that for claim 1. Namely, that *Armacost et al.* teaches a same pattern for a bottom conductive layer, dielectric layer, and top conductive layer.

As in the case of claim 1, Applicants believe such an interpretation of the reference is also erroneous. *Armacost et al.* does not show or suggest top and bottom conductive layers with the same pattern as a dielectric layer.

The metal-insulator-metal capacitor of *Armacost et al.* includes a capacitor dielectric layer (120) formed between a bottom plate layer (110) and a top plate layer (130). As shown in FIG. 7 of *Armacost et al.*, these three layers are clearly shown as each having different patterns.



Accordingly, because the reference relied upon by the rejection shows a top plate (130), capacitor dielectric (120), and bottom plate (110) of all different patterns, Applicants do not believe the combination of references can be construed as showing or suggesting a "bottom conductive layer, dielectric layer, and top conductive layer having the same pattern", as recited in claim 5. Absent such a showing, a prima facie case cannot exist.

For this reason, claim 5 is believed to be separately patentable.

For all of these reasons, this ground for rejection is traversed.

Rejection of Claim 23 Under 35 U.S.C. §103(a), based on *Hashimoto et al.* in view of U.S. Patent No. 6,104,053 (*Nagai*).

Claim 23 is directed to a memory cell that includes a first data storage node, a second data storage node, and a capacitor. The capacitor comprises a first plate coupled to the first data storage node, a second plate coupled to the second data storage node, and a third plate separated from the first and second plates by a capacitor dielectric. The memory cell also includes a

plurality of wiring portions, each comprising a commonly patterned first conductive layer and dielectric layer. A first wiring portion forms the first plate and a second wiring portion forms the second plate. The dielectric layer forms the capacitor dielectric.

The cited combination of *Hashimoto et al.* in view of *Nagai* does not show or suggest all the limitations of claim 23.

As emphasized above, Applicants' claim 23 recites a capacitor first plate formed by a first wiring portion and a capacitor second plate formed by a second wiring portion where each wiring portion comprises a commonly patterned first conductive layer. Such an arrangement is not shown or suggested by the cited combination of references.

Nagai et al. shows capacitor plates formed by different layers, and so cannot show or suggest Applicants' claim 23 arrangement.[5] *Hashimoto et al.* shows a stacked capacitor having lower and upper electrodes, but such electrodes are not formed by wiring portions that each include "a commonly patterned first conductive layer". Rather, the upper and lower electrodes are explicitly described as being patterned from different polysilicon layers:

With respect to the first embodiment of the reference:

> Next, as shown in FIGS. 12 and 13, an n-type polycrystalline silicon film... is deposited... and is patterned... to form the lower electrode 16 of the capacitor element C. (*Hashimoto et al.*, Col. 15, Line 66 to Col. 16, Line 3).

> Next, as shown in FIGS. 16 and 17, the n-type polycrystalline silicon film having a thickness of about 50 nm is deposited... and is patterned... to form the upper electrode 19 of the capacitor element C. (*Hashimoto et al.*, Col. 16, Lines 24-29).

With respect to the second embodiment of the reference:

> After this, the n-type polycrystalline silicon film, deposited by the CVD method, is patterned to form the lower electrode 41 of the capacitor element C... (*Hashimoto et al.*, Col. 19, Lines 23-25).

> [A]n n-type polycrystalline silicon film... is subsequently patterned to form the upper electrode 42 of the capacitor element C. (*Hashimoto et al.*, Col. 19, Lines 38-40).

With respect to the third embodiment of the reference:

> Next, as shown in FIGS. 43 and 44, the polycrystalline silicon film, deposited by a CVD method, is patterned to form a lower electrode 51 of the capacitor element C. (*Hashimoto et al.*, Col. 24, Lines 52-54).
>
> After this, the n-type polycrystalline silicon film, a deposited by a CVD method, is patterned to form an upper electrode 53 of the capacitor element C. (*Hashimoto et al.*, Col. 24, Line 66 to Col. 25, Line 1)

With respect to the fourth and last embodiment of the reference:

> Next, as shown in FIGS. 55 and 56, the n-type polycrystalline silicon film deposited over the silicon nitride film 40 by the CVD method is patterned to form the lower electrode 61 of the capacitor element C. (*Hashimoto et al.*, Col. 27, Lines 45-48).
>
> The n-type polycrystalline silicon film deposited on the capacitor insulating film 18 by the CVD method is patterned to form the upper electrode 62 of the capacitor element C. (*Hashimoto et al.*, Col. 27, Lines 57-60).

Because the cited references *Hashimoto et al.* and *Nagai* both show capacitor plates formed with different layers, Applicants believe that this combination of references cannot be considered to show or suggest Applicants' different plates comprising a commonly patterned first conductive layer.

For these reasons, Applicants do not believe a prima facie showing of obviousness has been established, and this ground for rejection is traversed.

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[5] See *Nagai*, FIGS. 1 and 34, which show an electrode (11) formed from layers (7) and (6), an electrode (20) formed from layers (19 and 18), and an electrode (40) formed from yet a different layer.

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Claim 5 has been amended, not in response to the cited art, but to ensure proper antecedent basis for a claim term.

The present claims 1-3, 5-7 and 21-23 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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